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APPLICATION NOTE

Pentium® Processor With Voltage Reduction Technology:

Power Supply Design Considerations for Mobile Systems

June 1997

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CONTENTS

1.0. INTRODUCTION

As the mobile market segment has closed the gap to desktop performance with equivalent notebook performance, the challenges to the system designer have increased tremendously. As the performance requirements have increased, so have the power consumption requirements. This results in the need for careful attention to thermal design to mitigate the potentially higher temperature within the system, to power supply designs which can supply the higher current needs, and to good power management design to extend battery life to an acceptable level. The focus of this application note is the power supply design considerations.

With the addition of the Pentium® processor with Voltage Reduction Technology to the processor roadmap, Intel is able to offer the higher performance level of a 90-MHz Pentium processor at a lower power consumption level than the Pentium processor 610\75 MHz. This allows the Pentium processor notebook designs to migrate to a higher performance Pentium processor without requiring major changes to existing designs. This allows the Pentium processor to migrate into the subnotebook market, which requires lower power consumption processors as well. The Pentium processor with Voltage Reduction Technology achieves lower processor power consumption by lowering the core voltage required by the processor while maintaining compatibility to existing I/O and memory through a separate 3.3 volt supply. The major advantage provided by this splitting of processor voltage requirements is that existing Pentium processor thermal designs will accept the higher performance while requiring minimal or no thermal changes.

The notebook design areas affected by the splitting of processor voltages are in the design of power supplies, the layout of printed circuit boards and the type, quality and quantity of capacitive decoupling provided at the processor. This application note will discuss these areas and make recommendations to allow the designer to minimize the changes to existing designs. This note does not address platform issues such as chip set support, graphics controllers and memory improvements needed to support the faster 60-MHz bus of the Pentium processor 90\60 MHz.

This application note was written for mobile system designers planning to migrate from Pentium processor 610\75 MHz designs to the Pentium processor with Voltage Reduction Technology designs. It is assumed that the reader is familiar with the documents listed in the reference section. It is highly recommended that these be read and understood before using the information in this note since this application note builds on the foundation created by these reports. Section 2 defines the differences between the Pentium processor 610\75 MHz and Pentium processor with Voltage Reduction Technology and outlines the areas to be aware of while designing a system for a Pentium processor with Voltage Reduction Technology. Section 3 discusses power supply design considerations resulting from split voltage requirements between the core and I/O logic. Section 4 discusses the power plane design considerations associated with printed circuit board development for the Pentium processor with Voltage Reduction Technology. Section 5 discusses the requirements for bulk and high frequency decoupling at the processor for both the core and I/O logic. Section 6 summarizes the results of empirical measurements of V_{CC} tolerance using the capacitance values recommended in section 5.0.

Note

The data presented in this application note reflects studies on a selected system. It is recommended that the following information be used as a starting point for designing a Pentium processor with Voltage Reduction Technology system and that measurements be made on individual systems to ensure a robust design.

2.0. DIFFERENCES BETWEEN PENTIUM® PROCESSOR 610\75 MHZ AND PENTIUM® PROCESSOR WITH VOLTAGE REDUCTION TECHNOLOGY

The architecture and internal features of the Pentium processor with Voltage Reduction Technology are identical to the Pentium processor 610\75 MHz, thereby maintaining hardware and software compatibility. The Pentium processor with Voltage Reduction Technology is offered in two versions, 75\50 and 90\60 MHz where the Pentium processor 610\75 MHz was only available in 75\50 MHz version. The Pentium processor with Voltage Reduction Technology will use the same packaging, Tape Carrier Package (TCP), used for the Pentium

processor 610\75 MHz as well as the SPGA package. Experience gained in the manufacture of the Pentium processor 610\75 MHz TCP designs can be applied to a Pentium processor with Voltage Reduction Technology design.

The Pentium processor with Voltage Reduction Technology lowers processor power requirements by lowering the voltage required by the core logic of the processor. This results in an approximately 20 percent savings in power over the Pentium processor 610\75 MHz at the same frequency. The Pentium processor with Voltage Reduction Technology also separates the voltage required (V_{CC}) for core functions (2.9 volts) and that required for I/O functions (3.3 volts). The Pentium processor with Voltage Reduction Technology maintains the same V_{CC} tolerance as required on the Pentium processor 610\75 MHz for both the core V_{CC} as well as I/O V_{CC}.

The separation of the processor voltages puts new requirements on the power supply design, layout of PCBs and decoupling requirements at the processor. These areas will be covered in the next sections.

As processors migrate to lower and lower core voltages, it is important that power supply designs take into account this trend and provide flexibility in design to handle these future voltages. This will minimize changes required in the future.

3.0. POWER SUPPLY DESIGN CONSIDERATIONS

With the separation of V_{CC} between the processor core logic and I/O logic, an additional voltage regulator is required to supply the 2.9 volts required by the core. The load handling capability of this regulator will support the majority of the processor requirements (approximately 90 percent of total current) while the processor load handling requirement on the 3.3 volt regulator drops to approximately 10 percent of the total processor current requirement.

The designer can choose between two types of regulators to implement the required core voltage. Section 3.2 discusses the use of commonly available switching and linear regulators from Linear Technology Corporation and Maxim Integrated Products to supply this voltage. Regulators from other power supply vendors are also available.

3.1. Power Supply Current Requirements

The power supply current specifications are shown in the table below. This value should be used for power supply design. It was determined using a worst-case instruction mix and V_{CC} + 165 mV. Power supply transient response and decoupling capacitors must be sufficient to handle the instantaneous current charges occurring during transitions from stop clock to full active modes.

Table 1. Pentium® Processor with Voltage Reduction Technology Maximum Power Supply Current Specs

	Pentium® Processor 75 MHz	Pentium Processor 90 MHz
2.9 Volt Max $I_{CC}2$	2096 mA	2515 mA
3.3 Volt Max $I_{CC}3$	265 mA	318 mA

3.2. Voltage Regulator Options

To supply the additional voltage required for the core, designers have a choice of adding a linear or switching regulator to their design and regulating down from the battery output voltage. These two power supply regulators yield different ranges of efficiency. A linear regulator is much like a voltage divider which steps down the input voltage to a specified output level (e.g., from 12V or 5V to 2.9V). The maximum efficiency offered by a 5V to 2.9V linear regulator is 58 percent, as shown by the following equation:

$$Efficiency = \frac{Vout}{Vin} \times 100$$

$$= \frac{2.9V}{5.0V} \times 100$$

$$= 58\ \%$$

In this case, the remaining 42 percent is dissipated as heat. A switching regulator, however, generates an output voltage by pulsing the input voltage through a MOSFET switch and an inductor. Since there are no voltage divider-type losses as in a linear regulator and the AC switching losses are small, there is much less dissipated heat. Switching regulators commonly offer up to 95 percent efficiency. For this reason, it is recommended that a switching regulator be used to generate the 2.9 volt requirement of the core.

There are trade-offs for the increased efficiency. Switching regulators have a larger component count than linear regulators and also a higher cost. However, the efficiency of the switching regulator with its minimum power loss makes it more ideal for the mobile application.

A switching regulator and associated support components require approximately 1.5 square inches of board space to implement. The maximum current supplied by any design will depend on the supporting components used in the design. Most manufacturers supply a reference design to make the design process as easy as possible.

In providing the voltage source for the processor core, the power supply should be designed to provide this output by adding an additional regulator in parallel with the existing 3.3 volt source as indicated in Figure 1a. This will ensure the 2.9 volt regulator will not be affected by any inefficiencies in a previous regulation stage. Figure 1b is an example of an inefficient design since a cumulative effect results from the inefficiency of the 3.3 volt source being supplied to the input of the 2.9 volt regulator.

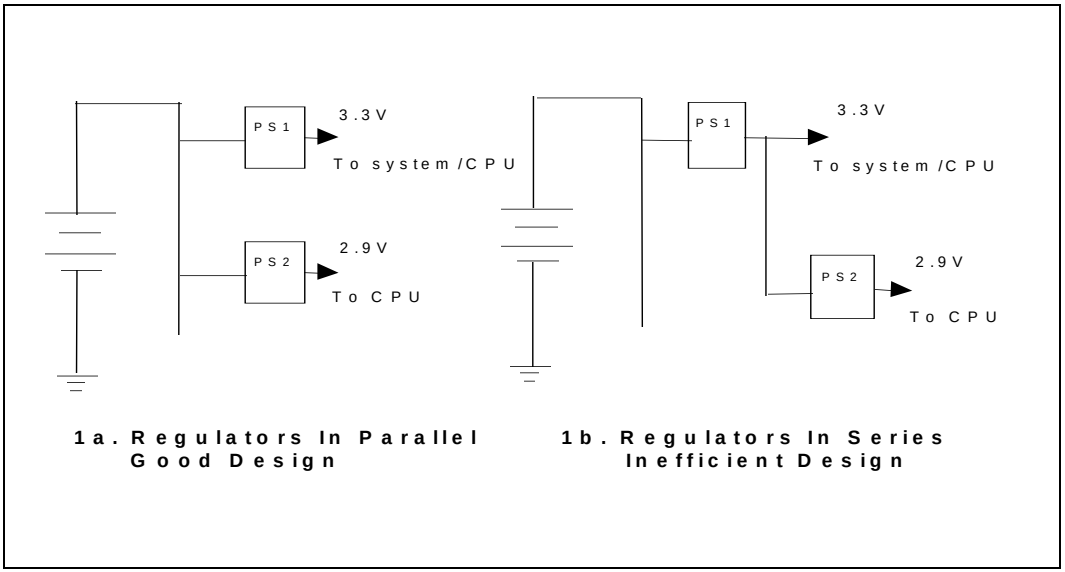

Figure 1. Examples of 2.9 and 3.3 Volt Regulators Connected in Parallel and in Series

Linear Technology Corporation and Maxim Integrated Products offer switching regulators that can be designed into power supplies meeting the maximum current and V_{CC} tolerance specifications of a Pentium processor mobile system (see Appendix C for vendor information). Other solutions may also be available from additional power supply vendors.

4.0. PCB LAYOUT CONSIDERATIONS

In most Pentium processor system board designs, the 3.3 volts for the processor is supplied on the board through a dedicated layer. With the requirement for a new 2.9 volt supply for the processor, it is not necessary to add a completely new power supply layer to the circuit board. It is possible to create a 2.9 volt "island" around the processor in the existing 3.3 volt power plane. The "island" needs to be large enough to include the processor, the required power supply decoupling capacitance (see section 5.0), and the necessary connections to the 2.9 volt source. The power supply regulator should be physically close to the processor.

Figure 2 is an example of a TCP power plane which contains several power islands. A large core voltage island surrounds the TCP package completely on three sides and partially on a fourth. The remainder of the fourth side provides access to I/O voltage pins for creating an I/O voltage island. Similar techniques can be used on SPGA packages as well.

The 2.9 volt voltage source, along with the desired amount of bulk and high frequency capacitance, should be located close to the processor to minimize inductance due to trace length. Trace widths should be kept as wide as possible to provide maximum current capability with minimal inductance.

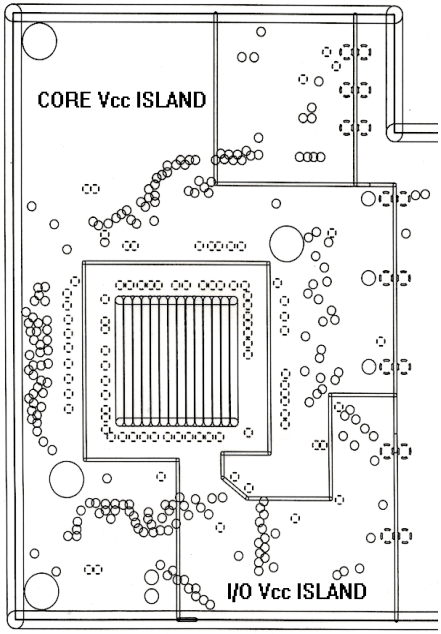

Figure 2. TCP Power Plane with Power Islands for Core and I/OV_{CC}

5.0. PROCESSOR CAPACITIVE DECOUPLING

Processor power supply decoupling is critical for reliable operation. There are two areas that the designer needs to address: high frequency decoupling resulting from small current changes in very fast transition periods (1-10 nS) and lower frequency decoupling resulting from large current changes in fast transition periods (50-300 nS).

The *Pentium® Processor 610\75 MHz Power Supply Considerations for Mobile Systems* application note indicates that the processor experiences rapid current changes transitioning between active operation and low power operation (Auto Halt Powerdown mode or STOP Grant state). These transitions occur in less than 100 nS with as much as 2.0 A in current change. Even during active operation, large current changes can occur from clock cycle to clock cycle, depending on the instruction mix of the application being executed. These rapid current changes result in large load changes to the power supply. When such load transients occur, current must be supplied from the power supply decoupling capacitors, since the power supply cannot change its output current instantly. Negative transients (voltage droop) occur when current load increases, while positive transients (voltage surges) occur when load current decreases.

The response time of a switching regulator power supply to a large transient current is limited by the value of the energy storing inductor, and is typically on the order of 10 uS or less. Adequate bulk capacitance, located as close as possible to the processor, is needed to provide current until the power supply can respond to the change in load. Capacitors with low ESR and ESL values are required to keep the processor supply voltage within the V_{CC} tolerance spec. Suggestions for the type and quantity of bulk decoupling capacitors to be used are provided in Section 5.1. The voltage transients caused by the rapid transitions between active and low power modes are additive to any DC voltage drops between the power supply regulator and the processor. Minimizing board level DC drops provides more margin for transient effects. This can be accomplished by using short, wide power traces to minimize resistance and inductance.

Due to the high internal speed of the processor and rapid transitions on the external bus, high frequency decoupling is also required. High frequency capacitors connected between the power and ground planes near the processor are required to filter these high frequency components of noise. Section 5.2 provides recommendations for the type and quantity of high frequency decoupling capacitors to be used.

5.1. Bulk Decoupling

As pointed out in Section 5.0, bulk decoupling is required with the Pentium processor, since the processor switches between normal and low power states very quickly, causing large instantaneous current changes. The resulting power supply voltage transient is illustrated in Figure 3.

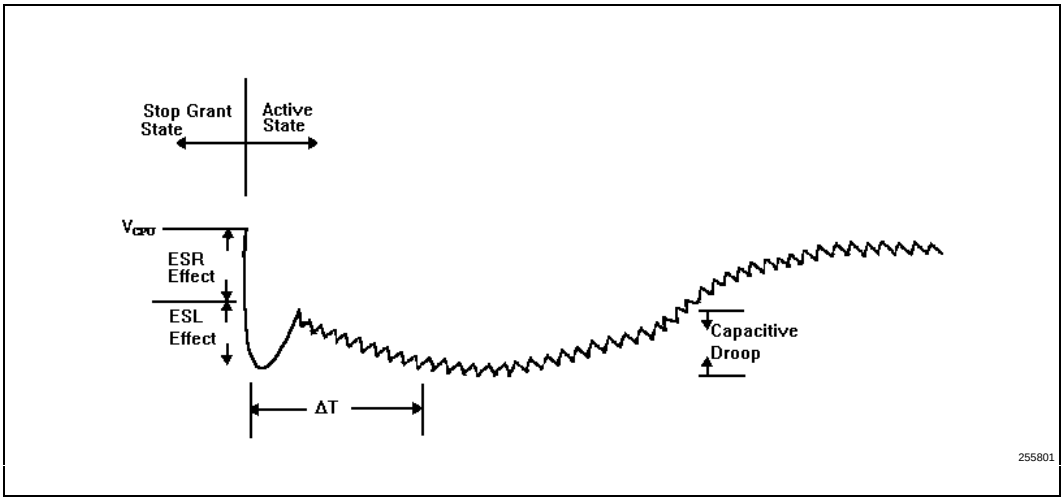

Figure 3. Example of Power Supply Voltage Transient

The voltage initially drops as the current encounters the decoupling capacitor's equivalent series resistance (ESR) and further undershoots by a voltage equal to the decoupling capacitor's equivalent series inductance (ESL) times the rate of change of current (di/dt). Then as the decoupling capacitor discharges, the power supply voltage droops until the power supply regulator reacts and is able to supply the full processor current. Since the processor is now active, high frequency noise also appears on the waveform. The system then settles to the initial voltage regulator setting, offset by any DC voltage drop. The total voltage dip must not exceed the voltage tolerance spec.

Part of the voltage tolerance specification is consumed by regulator tolerance (±2 percent), high frequency noise and any board level DC drops. The remaining amount is available to handle the processor active/low power transitions. Allocating about 1/2 of this amount for the ESR drop and the other 1/2 for the ESL undershoot and capacitive droop results in reasonable required values of ESR and ESL. If we allow too much for ESR, then the budget for ESL becomes prohibitive.

The following examples show how to determine the required component values, using a 60/40 ratio for ESR to capacitive droop. The solution can be fine-tuned to meet design requirements by adjusting the ratio between ESR and capacitive droop.

Core Supply Example

Power source: Lithium ion battery, 5.5 volts.

Switching regulator: 300 KHz, Vin = 5.5 volts, Vout = 2.9 volts, buck inductor L = 7.5 uH

ΔI = (Max active I_{CC} - Stop Grant I_{CC}*) for core V_{CC} pins

= 1.95 amps Pentium processor 90 MHz with Voltage Reduction Technology

= 1.78 amps Pentium Processor 75 MHz with Voltage Reduction Technology

ΔT = Regulator response time (ΔI = 1.95 amps, L = 7.5 uH) = 7 uS

ΔV = Voltage budget for ΔI

= V_{CC} tolerance specification (165 mV) - Regulator tolerance (2 percent) - high frequency noise (20 mV)*

= 165 mV - 2.9V x (0.02) - 20 mV = 87 mV

= $\Delta V_{ESR} + \Delta V_{CAPDROOP}$

*** Adequately decoupled high frequency noise measures about 40 mV peak-to-peak.**

Assume that the board DC drop is negligible.

Maximum allowable ESR:

$$ESR_{MAX} = \Delta V_{ESR} / \Delta I$$

Bulk decoupling can be calculated as:

$$C_{MIN} = (\Delta I \times \Delta T) / \Delta V_{CAPDROOP}$$

Allocating 60 percent of ΔV for ESR effects (ΔV_{ESR} = (0.6) x 87 mV, $\Delta V_{CAPDROOP}$ = (0.4) x 87 mV) gives the following results:

$$ESR_{MAX} = 0.027 \text{ ohm}$$

$$C_{MIN} = 392 \mu F$$

Note the low ESR value required for this application. This will require multiple low ESR capacitors in parallel to achieve this value. In this example, 4 x 100 µF / 0.1 ohm ESR capacitors will satisfy both maximum ESR and minimum bulk decoupling requirements.

This has now ensured that the maximum power supply voltage droop will not exceed the processor voltage tolerance specification for transitions between active and Stop Grant states. An additional factor that must also be comprehended is the inductive undershoot resulting from the rapid rate of current change times the ESL of the decoupling capacitors. As the processor resumes activity, there are many large, instantaneous demands for power supply current as the various internal circuits start switching. There is a need to ensure that the resulting change in power supply voltage remains within limits. Since this inductive voltage effect is additive to the ESR drop, its magnitude must be less than or equal to the capacitive droop.

Maximum allowable ESL:

$$ESL_{MAX} = (\Delta V_{ESL} \times \Delta T) / \Delta I$$

where

ΔV_{ESL} = voltage drop across the capacitor due to parasitic inductance

ΔI = current change within a specified ΔT

ΔT = period in which current changes

A current slew rate of 40 mA / nS will be used for this calculation. With 40 percent of the previously calculated 87 mV budget as the maximum allowed value for ΔV, an overall ESL of less than or equal to 0.87 nH is needed.

$$ESL_{MAX} = (0.4) \times 87 \text{ mV} / (40 \text{ mA / nS}) = 0.87 \text{ nH}$$

Surface mount capacitors with short lead lengths are available with an ESL value of 2 nH. Since four capacitors in parallel are needed to achieve the required overall ESR value, using these 2 nH ESL capacitors will result in an overall value of 0.5 nH, and will meet the overall requirement with margin left over for any additional inductance due to board traces.

I/O Supply Example

Switching regulator: 300 KHz, Vin = 5.5 volts,
Vout = 3.3 volts,
buck inductor L = 7.5 uH

ΔI = IO supply current

= 318 mA Pentium processor 90 MHz with Voltage Reduction Technology

= 265 mA Pentium Processor 75 MHz with Voltage Reduction Technology

ΔT = Regulator response time
(ΔI = 318 mA, L = 7.5 uH) = 3.0 uS

ΔV = Voltage budget for ΔI

= V_{CC} tolerance specification (165 mV) - Regulator tolerance (2 percent) - high frequency noise (20 mV)[1]

= 165 mV - 3.3V x (0.02) -20 mV = 79 mV

= $\Delta V_{ESR} + \Delta V_{CAPDROOP}$

[1] High frequency noise (about 40 mV peak-to-peak) from other devices on the 3.3 volt supply. Assume that the board DC drop is negligible.

Note:

This calculation is for the Pentium processor I/O supply bulk decoupling only. Other high power components, including the L2 cache, may require additional bulk decoupling to meet voltage tolerance specs for transitions between active and Stop Grant states.

Maximum allowable ESR:

$$ESR_{MAX} = \Delta V_{ESR} / \Delta I$$

Minimum bulk decoupling:

$$C_{MIN} = (\Delta I \times \Delta T) / \Delta V_{CAPDROOP}$$

Allocating 60 percent of ΔV for ESR effects (ΔV_{ESR} = (0.6) x 79 mV, $\Delta V_{CAPDROOP}$ = (0.4) x 79 mV) gives the following results:

ESR_{MAX} = 0.150 ohm $\qquad$ C_{MIN} = 30 µF

Again, please note the significance of low ESR. Use a 33 µF / 0.15 ohm ESR capacitor.

The current transients associated with I/O pin switching are small relative to the processor core and also much faster. Small, high frequency capacitors are needed to handle these current demands. The bulk decoupling capacitor is less important in this respect, and so there is no specific calculation of required ESL. Regardless, low ESL (short lead, surface mount, ESL = 2 nH) capacitors are recommended for I/O supply bulk decoupling.

Table 2. Pentium® Processor with Voltage Reduction Technology Bulk Decoupling Estimates (300-KHz Regulator)

	Pentium® Processor 75 MHz	Pentium Processor 90 MHz
2.9 Volt Core Decoupling	4x 100 µF / 0.1 ohm ESR / 2 nH ESL	4x 100 µF / 0.1 ohm ESR / 2 nH ESL
3.3 Volt I/O Decoupling	33 µF / 0.15 ohm ESR / 2 nH ESL	33 µF / 0.15 ohm ESR / 2 nH ESL

5.2. High Frequency Decoupling

High frequency decoupling is also critical for reliable operation. High frequency transients can be minimized by the use of multiple 1.0 µF and 0.01 µF bypass capacitors. Ceramic high frequency capacitors have the best high frequency performance and should be placed as close as possible to the processor between the processor power and ground pins. As a first approximation it is recommended that in a Pentium processor with voltage reduction technology design, the number of high frequency capacitors to be used should be equivalent to the number of capacitors used in a Pentium processor 610\75 MHz design. These capacitors should be split between the core V_{CC} and I/O V_{CC}.

In the testing to be described in the next section, it was found that using eight ceramic capacitors on the core V_{CC} and eight ceramic capacitors on the I/O provided adequate high frequency decoupling to maintain V_{CC} tolerance limits.

6.0. EXPERIMENTAL VERIFICATION OF CAPACITANCE ESTIMATES

A 90-MHz Pentium processor was used to verify the performance of the processor bulk capacitance recommendations. The 2.9V to the core was supplied by a 300-KHz switching regulator, and the 3.3V was supplied to the I/O by another 300-KHz switching regulator.

The method of measuring worst-case transients used for the experiments required the assertion of the STPCLK# input pin. Mobile chip sets provide support for STPCLK# control through programming a register which toggles STPCLK#. Oscilloscope probes were connected to STPCLK#, $V_{CC}2$ (core V_{CC}), $V_{CC}3$ (I/O V_{CC}) and STPCLK# was used as the trigger source.

Since the STPCLK# pin is toggled through the chip set hardware or by using a pulse generator connected to processor STPCLK# pin, additional software can be executed by the processor to produce high load conditions. DOS Edit with menu pulldown is an example of code which causes steady state high power consumption by the processor (about 5.1 W for the Pentium processor 90 MHz, depending on the system configuration). DOS Edit was used for these experiments. A high-power, FPU-intensive code loop can also be acquired from Intel (contact your local Intel sales representative) which will provide similar results. It should be noted that in making a measurement, sufficient time should be allowed to elapse before the power state is toggled. For example, a 300-KHz switching regulator typically takes about 7 µs to respond to a load change. If the power state is toggled before 7 µs, the overall response of the regulator cannot be viewed since the regulator has not had adequate time to respond.

The following discussions cover three different configurations of decoupling/filtering capacitance applied around the core and I/O V_{CC} pins of the Pentium processor on the daughter card. The first of these traces (Figure 4 below) illustrates the results from the recommended capacitance configuration and shows the overall pattern of STPCLK# used to drive the experiments.

The middle signal in Figure 4 is the I/O V_{CC} and the upper signal is the core V_{CC}. Note that the core voltage increases by 80 mV to 90 mV in the STPCLK# active (low) region, since the current drawn is greatly reduced, and thus so are the voltage drops along the power buses. (In our experimental setup, we had greater resistance in the power busses than recommended for production systems, and thus larger

DC offsets between the power states.) Also as expected, the noise level on the V_{CC} pins is reduced in the STPCLK# active region, especially for the core V_{CC}, since the core activity is essentially turned off and most of the noise on the core V_{CC} pins is generated inside the processor itself.

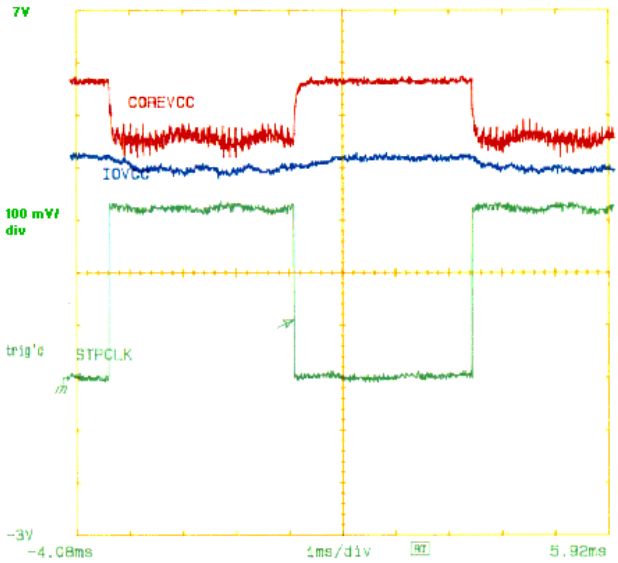

Figure 4. Example of Adequate Bulk Decoupling Capacitance for Core and High Frequency Capacitance

Using the recommended capacitance:

Bulk capacitors: core: 4 - 100 µF, I/O: 1- 47 µF

High frequency capacitor: core: 6 - 0.1 µF, 2 - 0.01 µF, I/O: 2 - 0.1 µF, 6 - 0.01 µF

The example system always operates within V_{CC} specifications and always works reliably. The largest variation from core V_{CC} minimum to maximum (peak-to-peak variation, including the DC offset) is about 150 mV peak-to-peak, which is well within the 214 mV tolerance (core V_{CC} tolerance - core regulator tolerance). The largest peak-to-peak variation in the I/O V_{CC} is about 50 mV, which is also well within the 198 mV tolerance (I/O V_{CC} tolerance - I/O regulator tolerance). (Note that in a production model, more guardband would be obtained by reducing the DC offset between the power states.)

Figures 5 and 6 illustrate the transition into and out of the Stop Grant state with a finer time resolution. The time scale of 200 ns will allow viewing undershoot and overshoot if they occur. The pictures show that using the recommended capacitive decoupling, there is no significant V_{CC} overshoot when STPCLK# is asserted or undershoot when it is deasserted.

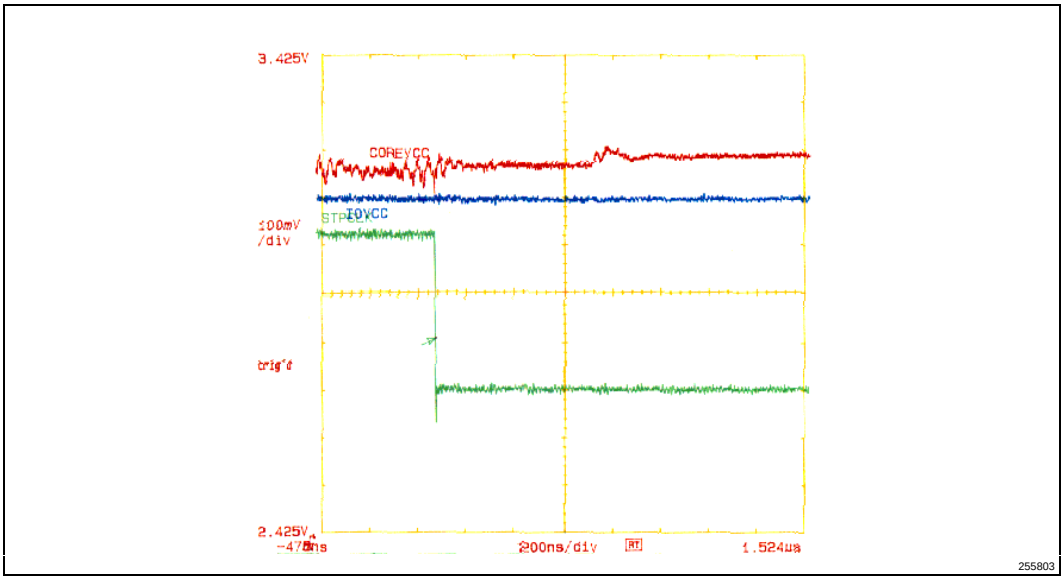

Figure 5. Example of Adequate Bulk Decoupling Capacitance for Core and I/O V_{CC} Entering Stop Grant

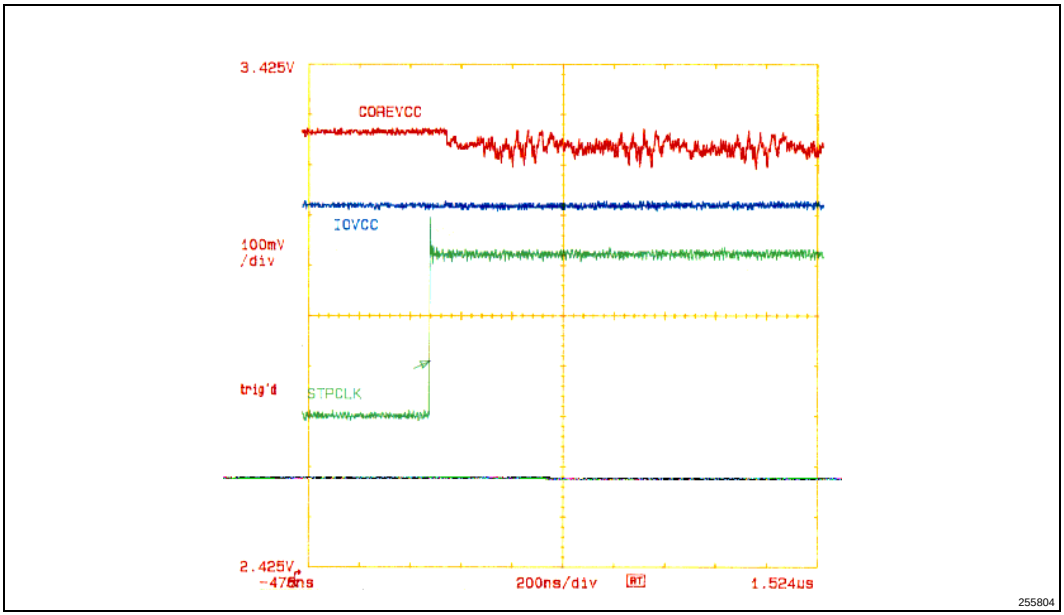

Figure 6. Example of Adequate Bulk Decoupling Capacitance for Core and I/OV_{CC} Exiting Stop Grant

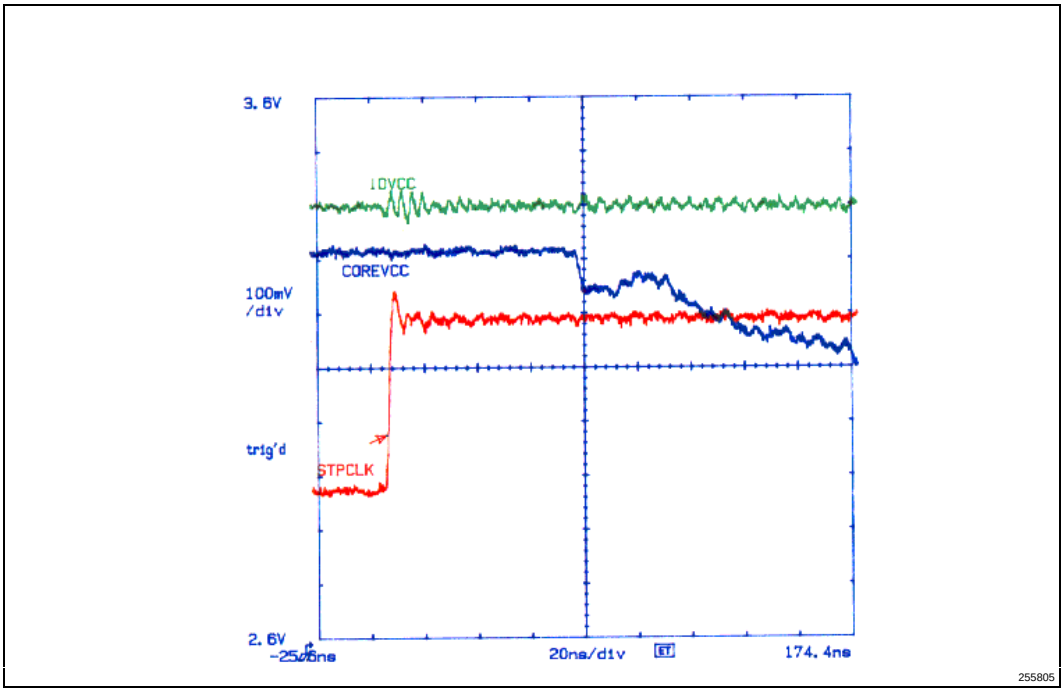

Figure 7. Example of No Bulk Decoupling Capacitance for Core and I/OV_{CC} Exiting Stop Grant

Using only high frequency filter capacitors:

Bulk Capacitors: 0; Standard high frequency filter Capacitors

Frequent large violations of specifications were observed on both I/O and core V_{CC}s. Figure 7 shows sizable ringing in the V_{CC} values after the processor enters the Stop Grant state with a peak-to-peak range of 210 mV on V_{CC} core, and about 65 mV on V_{CC} I/O. As expected, there is a severe droop in the core V_{CC} due to the lack of bulk capacitors to handle the abrupt change in load and the voltage tolerance specification is violated. The picture also illustrates the importance of the bulk decoupling for the core V_{CC}, where the largest load transients occur. Note also that although these experiments were done with no bulk capacitors added to the processor card, there was still capacitance in the power supply, small capacitance from loads and board effects, and a total of 0.88 µF from the high frequency capacitors.

Using *no* high frequency filter capacitors, with recommended bulk capacitors:

Bulk Capacitors: 400 µF core; 47 µF I/O.
High frequency Capacitors: None

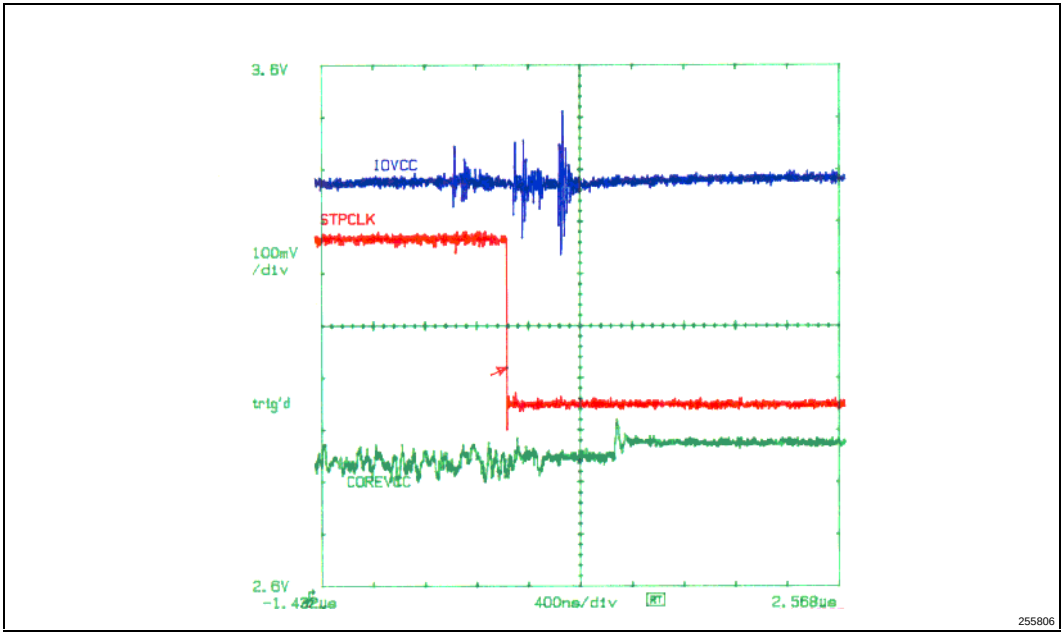

Figure 8. Example of No High Frequency Decoupling Capacitance for Core and I/O V_{CC} Exiting Stop Grant

A high magnitude of high frequency noise was observed on both the core and I/O V_{CC}. Figure 8 shows almost 300 mV of peak-to-peak noise on the I/O V_{CC}, and about 125 mV of peak-to-peak noise on the core V_{CC}. In this case, the system does not meet the voltage tolerance specifications and is not stable.

Note

The data presented in this application note reflects studies on a selected system. It is recommended that the following information be used as a starting point for doing a Pentium processor with voltage reduction technology system and that measurements be made on individual systems to ensure a robust design.

7.0. SUMMARY

With the addition of the Pentium processor 90 MHz to the microprocessors a designer has to choose from, additional design issues must be addressed. The separation of core and I/O voltages requires the use of an additional regulator to supply the 2.9 volt requirement of the core. This in turn requires the separation of power planes on the system board or daughter card. Appropriate decoupling of the core V_{CC} and I/O V_{CC} is also required to ensure the V_{CC} tolerance specifications are met.

Using power islands for core V_{CC} and I/O V_{CC} offer the designer an option to avoid using an additional power plane for the system board or daughter card. There are switching regulator controllers commercially available which can be used to design power supplies to source the worst case current for the Pentium processor with Voltage Reduction Technology. Transients during large current changes can be overcome by using adequate bulk decoupling capacitance. Additional high frequency decoupling will help reduce high frequency noise to an acceptable level. It is recommended that the bulk and high frequency capacitance estimates provided in this note, be used as a starting point for selecting the correct amount of decoupling used in a Pentium processor with Voltage Reduction Technology. It is further recommended that the V_{CC} tolerance for both core and I/O be verified through the use of applications (such as DOS Edit, and I/O intensive benchmarks) which provide a worst case operational scenario. This

will ensure that the final design will meet V_{CC} tolerance specifications.

APPENDIX A. EXPERIMENTAL PLATFORM

All measurement data and oscilloscope traces were taken on the following platform/test equipment:

Neptune* 82430 PCI Evaluation System
TCP-to-SPGA Converter Nehemiah Card
300-KHz Switching Regulator Power Supply
Tektronix* TLS216 Logic Scope (16 Channel, 2 Hz)
Tektronix Pulse Generator PG2011

APPENDIX B. REFERENCES

Pentium® Processor at iComp® Index 610\75 MHz **(Order Number 242323)†**

Pentium® Processor (610\75) Power Supply Considerations for Mobile Systems **Application Note, (Order Number 242415)**

AP517 Pentium® Processor (610\75) Power Consumption **Application Note, (Order Number 242416)**

AP515 Pentium® Processor (610\75) TCP System Thermal Design **Application Note, (Order Number 242414)**

APPENDIX C. VENDORS PROVIDING VOLTAGE REGULATORS AND CAPACITORS

The list below is meant to be representative only, and does not include all vendors of a particular type. Intel has not tested all of the components listed below and cannot guarantee that these components will meet every PC manufacturers specific requirements.

Voltage Regulators:

Linear Technology Corporation
1630 McCarthy Blvd.
Milpitas, CA 95035-7487
Tel. (408) 432-1900

Maxim Integrated Products
120 San Gabriel Drive
Sunnyvale, CA 94086
Tel. (408) 737-7600

Decoupling Capacitors:

AVX Corporation TPSE Series
Myrtle Beach, South Carolina 29577 USA

KEMET Electronics Corporation T Series
P.O.Box 5928
Greenville, South Carolina 29606 USA
Tel. (803) 963-6348

Nichicon (American) Corporation PL Series
927 East State Parkway,
Schaumburg, Illinois 60173 USA

Sanyo Video Components OS-CON Series
2001 Sanyo Ave.
San Diego, California 92073 USA
Tel. (619) 661-6835